CPRE 4920 Status Report 03

2/12/2025 – 02/26/2026

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Cache Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

  Since the last status update, we finished the core design and made major progress on the core controller design. We have also started integration of all of our top level components.

- **Past Week Accomplishments**

  - Colin McGann: Fixed perspective scaling on rasterizer. Integrated cores and rasterizer. Got output from system using an index buffer.
  - Jack Tonn: I finished the core HDL and passed it through merge requests. I also started updating the design document to reflect the changes that I made with the core.
  - Dawud Benedict: Completed Cache design and passed all unit tests (while SRAM set to functional), started exploring hold violation errors and synthesis.
  - Michael Drobot: Completed index fetcher testing. Completed dispatcher testing. Completed core controller design, testing, and synthesis, passes test_core.s.
  - Sam Forde: Rewrote model of off-chip SPI SRAM behavioral Verilog model used for testing. This was to pin down errors in our SPI controller, which has had issues. Also provided assistance with implementing SRAM into the cache.

- Josh Arceo: Tweaked area optimizer, got openlane running on my home pc to relieve load off of comparch, optimized multiple modules, created a table of areas to begin getting a rough estimate of how much die area we are taking up, started new hardware module: fragment fifo
- Emil Kosic: Went through multiple design iterations of wb to pk bridge and wrote hdl for half of its functionality. Began testing the module itself in simulation with other modules

- **Pending Issues**
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- **Individual contributions**

NAME	Individual Contributions	Hours this period	HOURS cumulative
Colin McGann	Integrated top level, fixed texture scaling for rasterizer	60	310
Jack Tonn	Core implementation & testing & design doc	40	240
Dawud Benedict	Finished cache	25	138
Michael Drobot	Core controller complete (including submodules)	60	322
Sam Forde	Rewrote SPI SRAM chip behavioral model	18	113
Josh Arceo	Optimization on home pc, table entires, startedfragment fifo	18	105
Emil Kosic	Wb to pk brdige design, rtl and testing	30	126

- **Plans for the upcoming weeks**
  - Colin McGann: Work on integrating the core controller and getting a working FPGA model
  - Jack Tonn: Core design doc and required functional changes
  - Dawud Benedict: Synthesize Cache and look into hold violations. Test on the FPGA, then help with integration.
  - Michael Drobot: Integration, multicore test, and adding commercial SRAM into core controller.
  - Sam Forde: Use rewritten SRAM chip model to find errors, and provide assistance with other parts of project.
  - Josh Arceo: Finish and test fragment fifo
  - Emil Kosic: Complete, test, synthesize wb to pk bridge